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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,226	01/14/2004	Raymond J. Blasko	DP-310692	3255

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EXAMINER	
CARPIO, IVAN HERNAN	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,226	BLASKO ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-13* is/are allowed.

6)☒ Claim(s) *1-7,14,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's first argument with respect to independent claims 1 and 14 is that neither Asao or Kameyama disclose a face seal is compressed between the insulator block and the lower surface of an upper housing, and furthermore that Kameyama teaches away from combining Asao with Kameyama, examiner respectfully disagrees. Examiner agrees that neither Asao nor Kameyama, independently teaches a face seal is compressed between the insulator block and the lower surface of an upper housing, but the question is not whether they teach the aforementioned limitation independently but whether in combination they teach the aforementioned limitation. The combination is in fact the face seal and the insulator block, as taught by Kameyama, in place of the resin block, as taught by Asao, thereby placing a face seal compressed between the insulator block and the lower surface of the upper housing, in view of this it is evident that Kameyama does not teach away from Asao. All remaining arguments are moot in view of new rejection necessitated by amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asao (US Patent 6244877) and Kameyama (US Patent 6616480).

With respect to claim 1, Asao teaches an electrical assembly comprising, a lower housing (column 4, lines 41-42), a circuit board (figure 1, element 4 and column 6 lines 15 and 16) mounted in the lower housing an insulator block (figure 1, element 12) mounted on and in contact with an upper surface of the circuit board (figure 1, element 12), holding a plurality of conductive terminals (figure 1, elements 13a), so that the terminals have contact heads extending above a top surface of the insulator block and connector tails extending below a bottom surface of the insulator block and attached to the circuit board, upper housing (figure 1, element 2a) having an upstanding shroud (figure 1, element 5), means to attach the upper housing so that the contact heads of the terminals are disposed within the shroud (figure 1 and column 6 lines 15-17). Asao does not teach a face seal above the insulator block so that the contact heads of the terminals extend through the face seal and the face seal is compressed between the top surface of the insulator block and a lower surface of the upper housing. Kameyama teaches an electronic assembly (Fig. 5) with a face seal (Fig. 5, element 7) above an insulator block (Fig. 5, element 6) where the contact heads of terminals (Fig. 5, elements 5) extend through the face seal. It would have been obvious to one of ordinary skill in the art at the time of the invention to place a face seal, as taught by Kameyama, on top of an insulator block in an electronic assembly (thus between the insulator block and upper housing), as taught by Asao, for the purpose of protecting the circuits inside the housing from dust, moisture and other damaging outside elements.

With respect to claim 2 and in accordance with claim 1, Asao teaches that the shroud has an outer periphery (Fig. 1, element 5) and the insulator block has an outer periphery (Fig.1, element 12) that is smaller than the outer periphery of the shroud.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asao in view of Kameyama and further in view of Uleski.

With respect to claim 14, Asao teaches an electrical assembly comprising, a lower housing (column 4, lines 41-42), a circuit board (figure 1, element 4 and column 6 lines 15 and 16) mounted in the lower housing an insulator block (figure 1, element 12) mounted on and in contact with an upper surface of the circuit board (figure 1, element 12), holding a plurality of conductive terminals (figure 1, elements 13a), so that the terminals have contact heads extending above a top surface of the insulator block and connector tails extending below a bottom surface of the insulator block and attached to the circuit board, upper housing (figure 1, element 2a) having an upstanding shroud (figure 1, element 5), the shroud having an outer periphery (Fig. 1, element 5) and the insulator block has an outer periphery (Fig.1, element 12) that is smaller than the outer periphery of the shroud. Asao does not teach a face seal above the insulator block so that the contact heads of the terminals extend through the face seal and the face seal is compressed between the top surface of the insulator block and a lower surface of the upper housing and doesn't teach that the upper housing is attached to the insulator block. Kameyama teaches an electronic assembly (Fig. 5) with a face seal (Fig. 5,

element 7) above an insulator block (Fig. 5, element 6) where the contact heads of terminals (Fig. 5, elements 5) extend through the face seal. It would have been obvious to one of ordinary skill in the art at the time of the invention to place a face seal, as taught by Kameyama, on top of an insulator block in an electronic assembly (thus between the insulator block and upper housing), as taught by Asao, for the purpose of protecting the circuits inside if the housing from dust, moisture and other damaging outside elements. It would have been obvious to one of ordinary skill in the art at the time of the invention to attach the upper housing to the insulator block, as taught by Uleski, in the electrical assembly, taught by Asao, because doing so more securely attaches the electrical assembly and increases the effectiveness of the seal.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabrisko (US 6413119) in view of Asao.

With respect to claim 1, Gabrisko teaches an electrical assembly comprising a circuit board (Fig. 1, element 14), an insulator block (Fig. 1, element 26 and 24) mounted on an in contact with an upper surface of the circuit board holding a plurality of electrically conductive terminals (Fig. 3, elements 20) so that the terminals have contact heads extending above the top surface of the insulator block and connector tails extending below a bottom surface of the insulator block and attached to the circuit board (column 2, lines 50-54), a face seal (Fig. 3, element 46) above the insulator block so

that the contact heads of the terminals extends through the face seal, and an upper housing (Fig. 3, element 12) having an upstanding shroud, and contact heads disposed within the shroud and the face seal is compressed between the top surface of the insulator block and a lower surface of the upper housing. Gabrisko does not teach a lower housing and that the circuit board is mounted in the lower housing. Asao teaches a lower housing (Fig. 4) and a circuit board mounted in the lower housing. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a lower housing, as taught by Asao, and to mount the circuit board in the lower housing for the purpose of protecting the circuit board from physical and atmospheric dangers.

With respect to claim 2 and in accordance with claim 1, Gabrisko teaches that the shroud has an outer periphery (Fig. 3) and the insulator block has an outer periphery that is smaller than the outer periphery of the shroud.

With respect to claim 3 and in accordance with claim 2, Gabrisko teaches that the terminals extend linearly from the contact heads to the connector tails and the smaller outer periphery of the insulator block provides a space beneath the upper housing for attaching electrical and/or electronic components to the circuit board adjacent the insulator block (Fig. 3, the space to the right and left of the insulator block 24).

With respect to claim 4 and in accordance with claim 2, Asao teaches the smaller outer periphery of the insulation block is spaced inwardly of the outer periphery of the shroud (figure 3).

With respect to claim 5 and in accordance with claim 3, Asao teaches the smaller outer periphery of the insulation block is space inwardly of the outer periphery of the shroud (figure 3).

With respect to claims 6 and 12, Gabrisko teaches that the means to attach the upper housing includes the upper housing being attached to the insulator block (column 3, lines 13-22).

With respect to claim 7 and in accordance to claim 1, Asao teaches that the means to attach the upper housing includes the upper housing being attached to the lower housing (column 6, lines 16 and 17).

With respect to claim 15 and 16 and with all the limitations of claims 6 and 12, Gabrisko teaches an electrical assembly that includes an insulator block with lateral extensions and wherein the means to attach the upper housing includes the upper housing being attached to the lateral extension (column 3, lines 13-22).

With respect to claim 14, Asao teaches an electrical assembly comprising, a circuit board (Fig. 1, element 14), an insulator block (Fig. 1, element 26 and 24) mounted on an in contact with an upper surface of the circuit board holding a plurality of electrically conductive terminals (Fig. 3, elements 20) so that the terminals have contact heads extending above the top surface of the insulator block and connector tails extending below a bottom surface of the insulator block and attached to the circuit board (column 2, lines 50-54), a face seal (Fig. 3, element 46) above the insulator block so that the contact heads of the terminals extends through the face seal, and an upper housing (Fig. 3, element 12) having an upstanding shroud, and contact heads disposed

within the shroud and the face seal is compressed between the top surface of the insulator block and a lower surface of the upper housing. The shroud having an outer periphery that is smaller than the outer periphery of the shroud. Gabrisko does not teach a lower housing and that the circuit board is mounted in the lower housing wherein the lower housing is attached to the upper housing. Asao teaches a lower housing (Fig. 4) and a circuit board mounted in the lower housing and that lower housing being attached to the upper housing. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a lower housing, as taught by Asao, and to mount the circuit board in the lower housing for the purpose of protecting the circuit board from physical and atmospheric dangers.

Allowable Subject Matter

Claims 8 – 13 contain allowable subject matter.

The following is a statement of reasons for the indication of allowable subject matter: There is simply no evidence in the prior art teaching or making obvious disposing a face seal with in a recess of the top surface of the insulator block as in the claimed combination.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IC

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